

Subject:

EAST - [1234.wsp:1]

File View Edit Tools Window Help

Drafts BRS: 3
BRS:
Pending
Active L1: (1) ("6694497").PN.
L2: (1) "20020002698".PN.
L3: (1) "6505342".PN.
L4: (1) "6031993".PN.
L5: (1) "5913023".PN.
L6: (1) "5437037".PN.
L7: (5724) hdl or vhdl
L8: (2714) coverage same state
L9: (88) 7 and 8
L10: (57) timing and signal and 9
L12: (63) state adj coverage
L13: (13) 10 and 12
L14: (196057) trace\$2
L15: (11) 12 and 14
L16: (30) verify\$7 and 12
L17: (4) trace and 16
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash

Search
DBs
Default operation
trace and 1

BRS form

U	I	Document ID	Issue Date	Pages	Title	Current OR	RC
1	Γ	US 6782518 B2	20040824	21	System and method for facilitating coverage feedback testcase	716/5	703
2	Γ	US 6484134 B1	20021119	13	Property coverage in formal verification	703/14	703
3	Γ	US 4945410 A	19900731	19	Satellite communications system for medical related images	725/67	358
4	Γ	US 4802008 A	19890131	18	Satellite communications system for medical related images	725/67	348

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File View Edit Tools Window Help

Drafts

- BRS:
- Pending
- Active
 - L2: (5743) vhdl or hdl
 - L1: (1751) state same signal\$1 same trace
 - L3: (29) 1 and 2
 - L4: (18) verify\$6 and 3
 - L5: (1) ("6694497").PN.
 - L6: (63) trace adj monitor
 - L7: (0) 2 and 6
 - L8: (0) hdl and 6
 - L9: (32) trace adj2 monitor
 - L10: (2) 2 and 9
 - L11: (1764) rostocker or dangelo
 - L12: (225) rostocker.in. or dangelo.in.
 - L13: (3) 1 and 12
 - L14: (0) 9 and 12
 - L15: (0) 6 and 12
 - L16: (32) trace and 12
 - L17: (12) monitor and 16
 - L18: (174) verification and 1
 - L19: (17) 2 and 18
- Failed
- Saved
- Favorites
- Tagged (0)
- UDC

BRS

U	Document ID	Issue Date	Pages	Title	Current OR	Current
1	<input checked="" type="checkbox"/> US 6826717 B1	20041130	20	Synchronization of hardware and software debuggers	714/39	714/725
2	<input checked="" type="checkbox"/> US 6732068 B2	20040504	51	Memory circuit for use in hardware emulation system	703/24	326/40; 703/23;
3	<input checked="" type="checkbox"/> US 6694464 B1	20040217	61	Method and apparatus for dynamically testing electrical	714/725	714/735 714/736
4	<input checked="" type="checkbox"/> US 6691287 B2	20040210	31	Functional verification system	716/4	703/14; 716/10;
5	<input checked="" type="checkbox"/> US 6678841 B1	20040113	16	Function test support system and function test support method and	714/57	714/33
6	<input checked="" type="checkbox"/> US 6629297 B2	20030930	30	Tracing the change of state of a signal in a functional verification	716/5	716/4; 716/7
7	<input checked="" type="checkbox"/> US 6625786 B2	20030923	30	Run-time controller in a functional verification system	716/5	716/1; 716/4;
8	<input checked="" type="checkbox"/> US 6510405 B1	20030121	17	Method and apparatus for selectively displaying signal	703/16	703/17; 714/37;
9	<input checked="" type="checkbox"/> US 6480988 B2	20021112	29	Functional verification of both cycle-based and non-cycle based	716/5	703/16
10	<input checked="" type="checkbox"/> US 6470480 B2	20021022	30	Tracing different states reached by a signal in a functional	716/4	324/528 324/758
11	<input checked="" type="checkbox"/> US 6377912 B1	20020423	55	Emulation system with time-multiplexed interconnect	703/28	716/1